LISA Pathfinder / SMART-2

Mid-way lessons learnt from the LTP development

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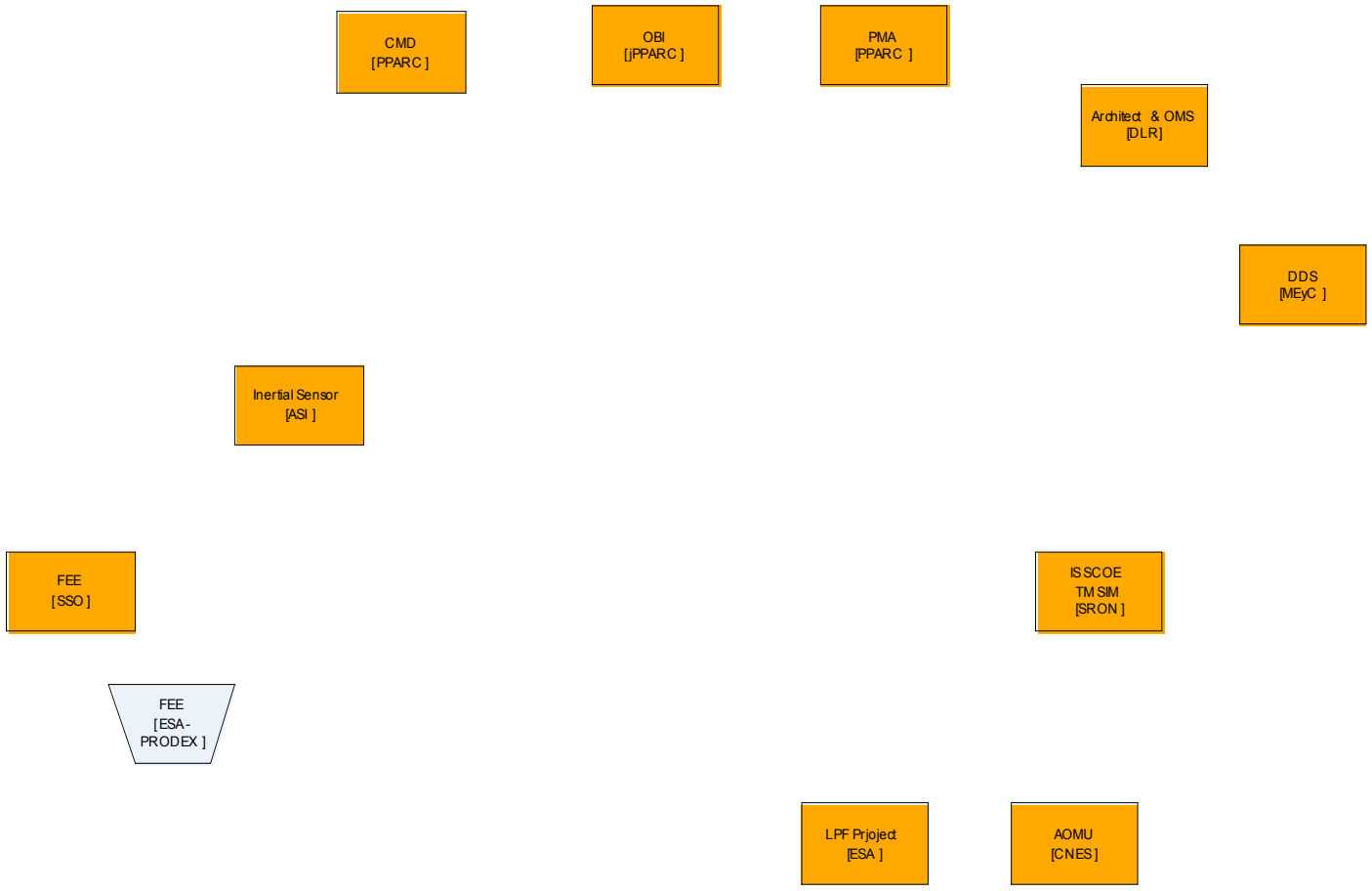
Summary

- Structure of the talk
  - Statement of the case
  - Something to keep in mind
  - *(My apologies for the over-simplification)*

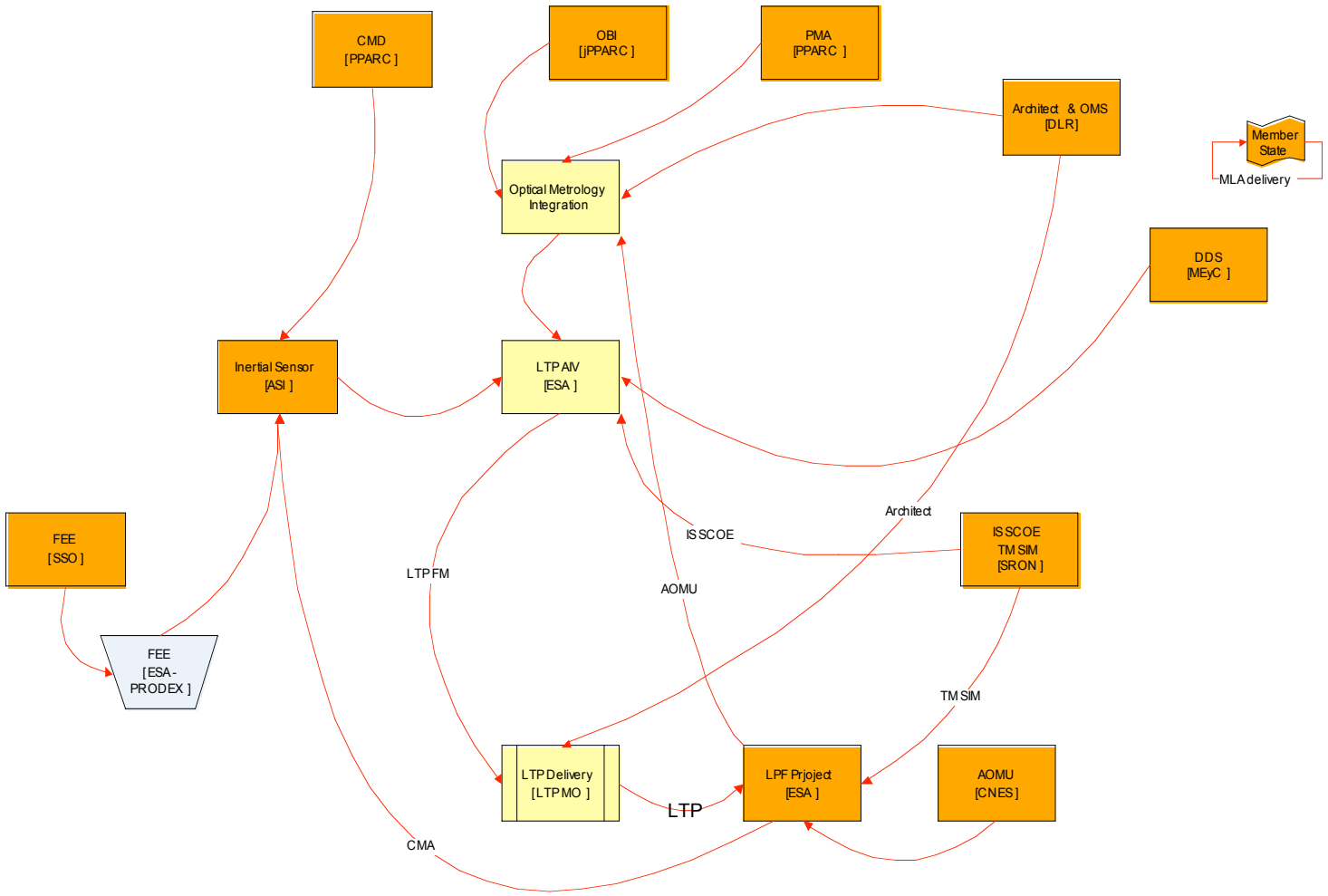
- There exists continuous communication LPF and LISA
  - Through PI's & Science Teams
  - The LISA Project Team has full visibility of LPF progress
  - The LPF Project Team has reviewed the MTR documents of the LISA Formulation Study
  - Through the main industrial partner, Astrium

Case 1: follow the hardware

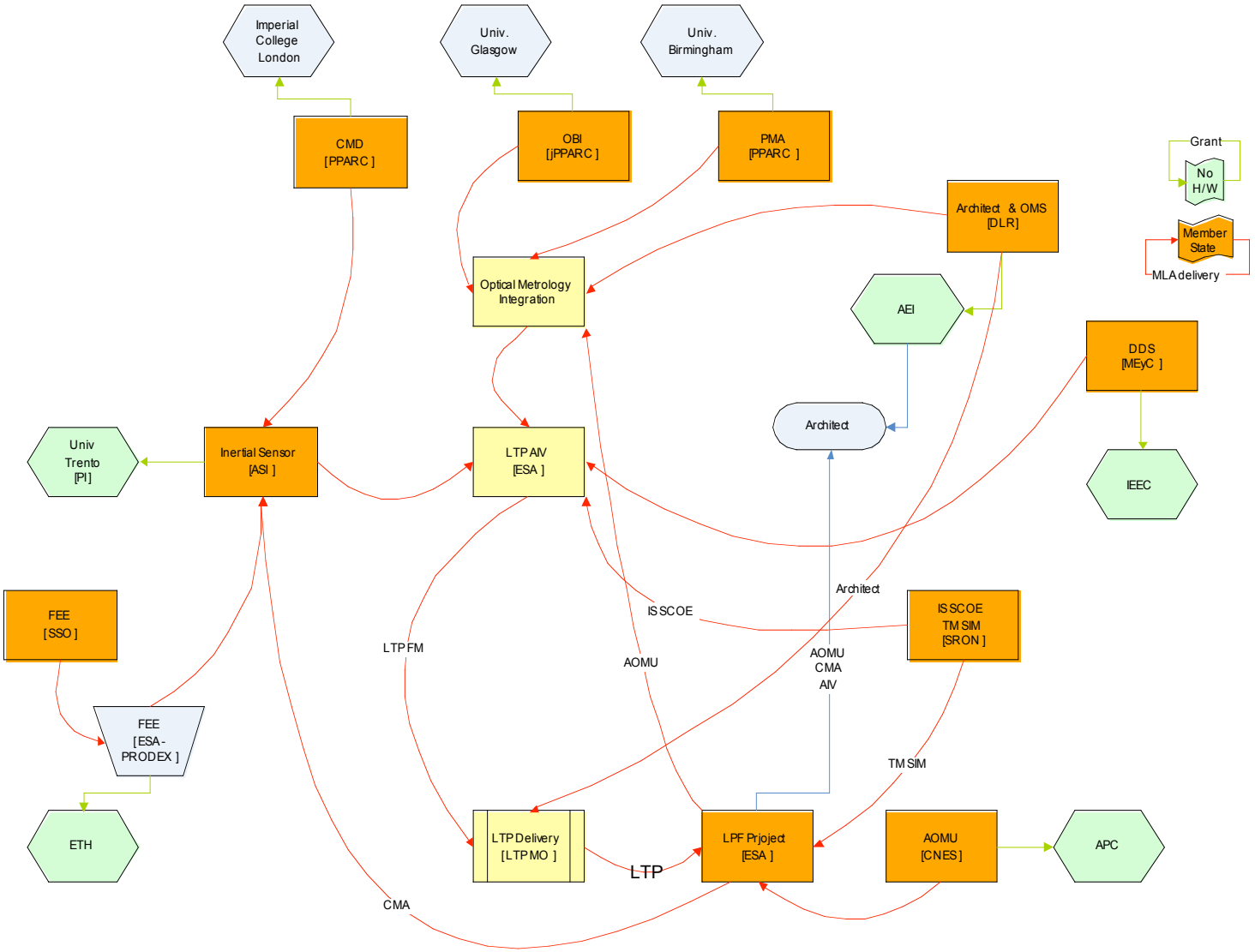
Contributing member states



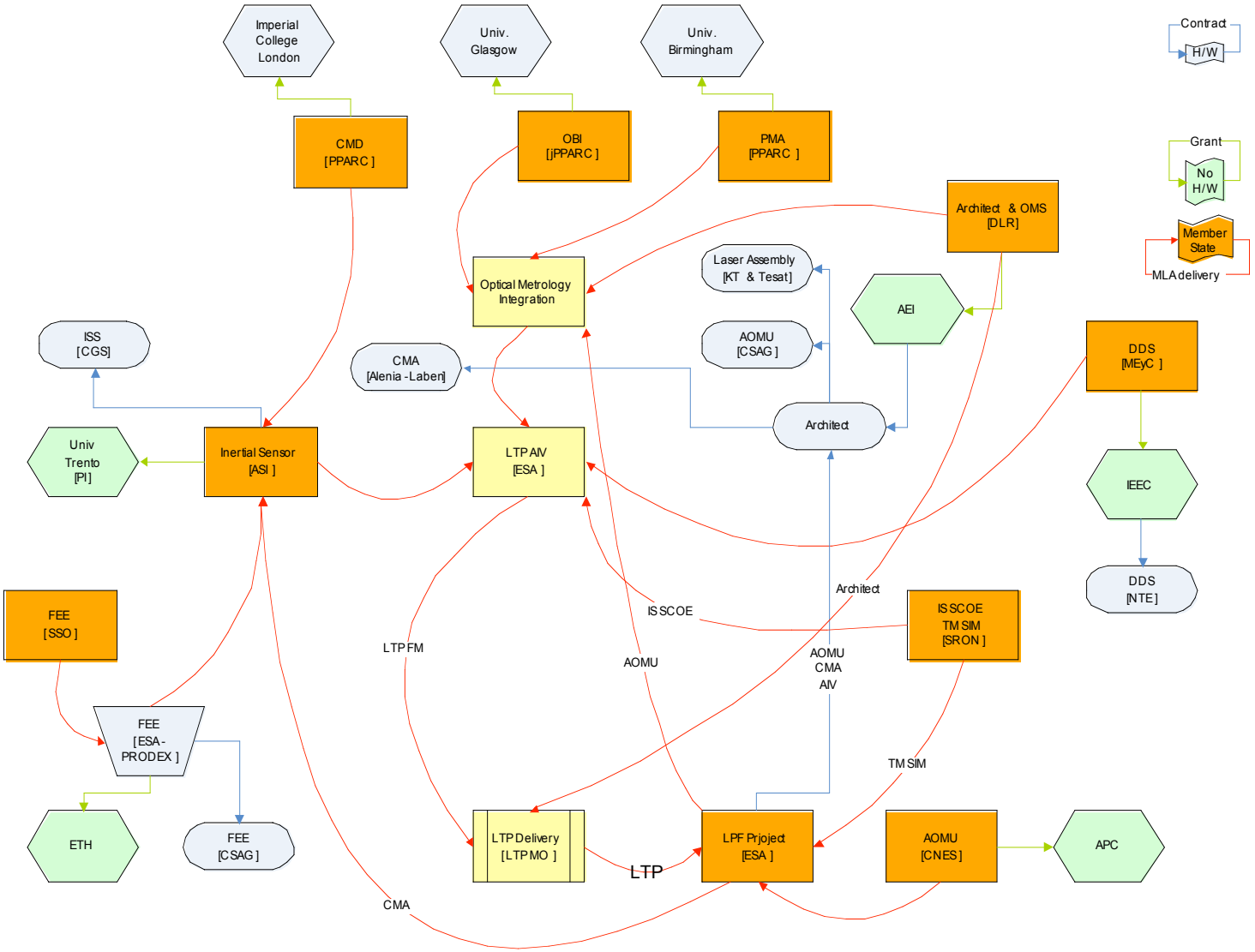
Multi-Lateral Agreement



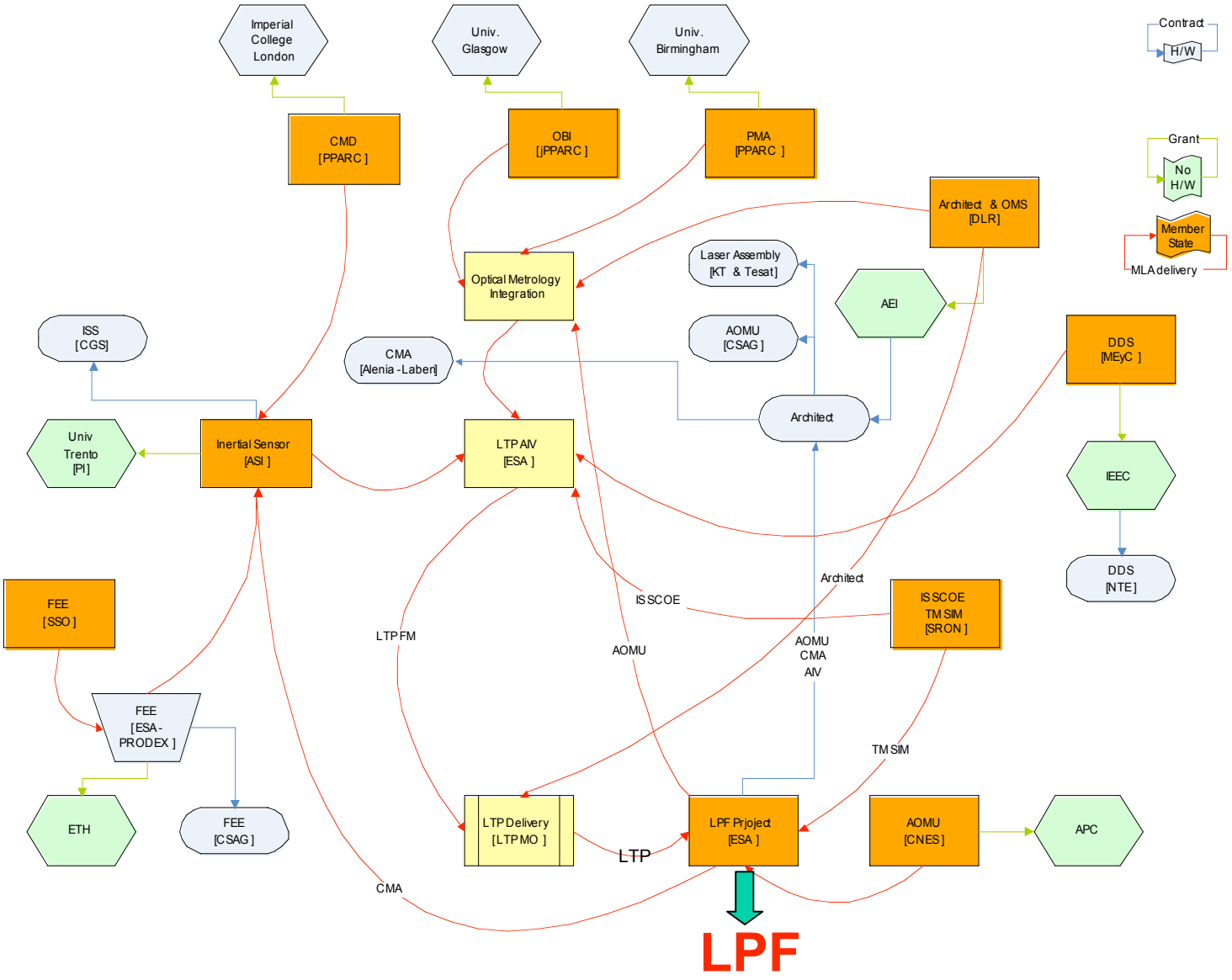
Main scientific institutes



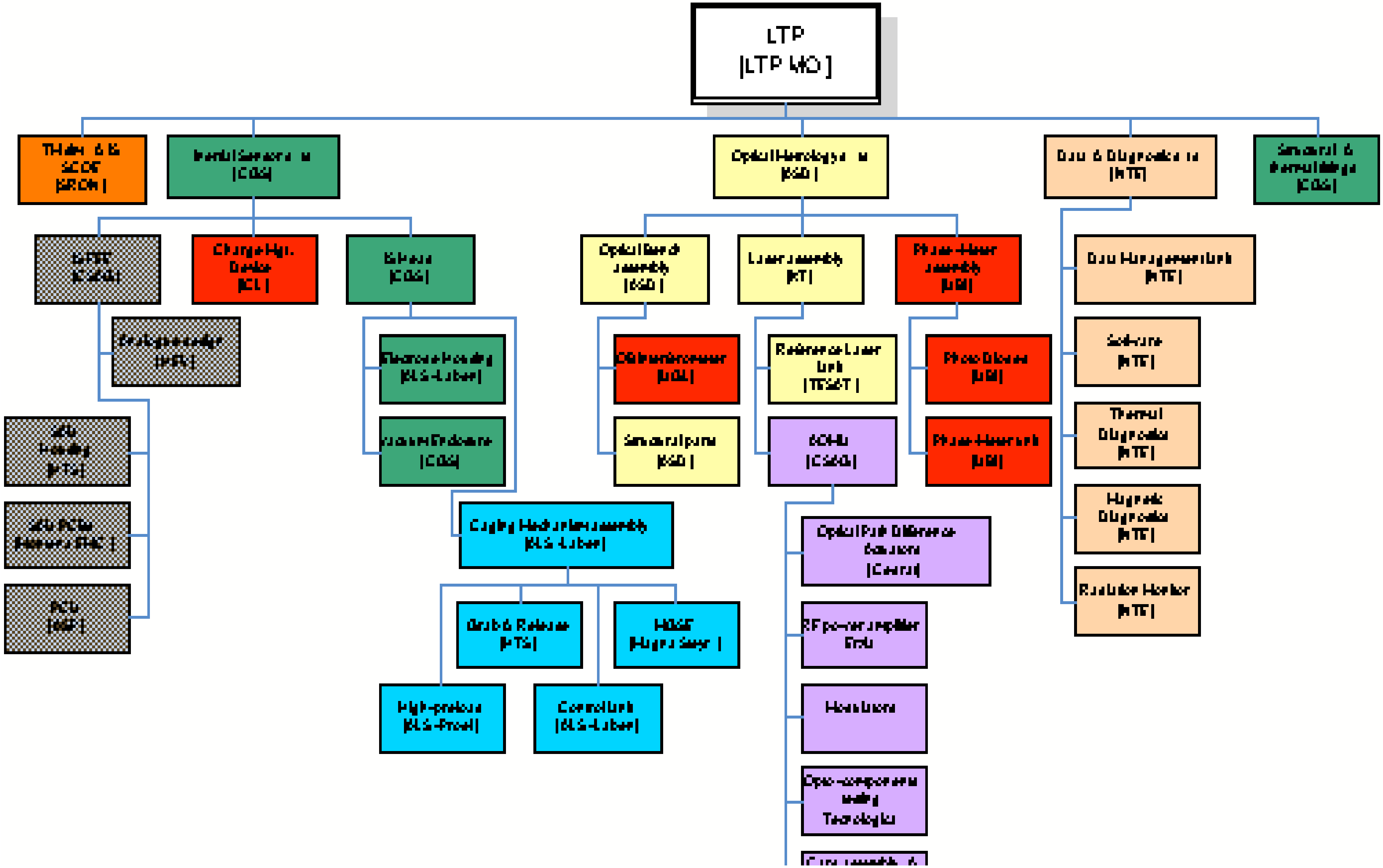
Main LTP Suppliers



The mission


Imperial College London
Univ. Glasgow
Univ. Birmingham
Contract
H/W
CMD [PPARC]
OBI [jPPARC]
PMA [PPARC]
Grant
No H/W
Architect & OMS [DLR]
Member State
MLA delivery
Optical Metrology Integration
Laser Assembly [KT & Tesat]
AEI
ISS [CGS]
AOMU [CSAG]
CMA [Alenia - Laben]
DDS [MEyC]
Architect
Univ Trento [PI]
Inertial Sensor [ASI]
LTP AIV [ESA]
IEEC
DDS [NTE]
FEE [SSO]
ISSCOE
ISSCOE TMSIM [SRON]
Architect
LTP FM
AOMU
AOMU CMA AIV
FEE [ESA - PRODEX]
TMSIM
ETH
FEE [CSAG]
LTP Delivery [LTP MO]
LTP
LPF Prjoject [ESA]
AOMU [CNES]
APC
CMA
LPF

LTP PFM tree



Lesson 1: keep it simple

- Tree-like organisation of work and product trees
- Interfaces are not only thermo-mechanical & electrical
  - Functional: two computers, two data buses
  - Verification: from over-testing to blurry responsibilities
  - System performance
- DFACS-LTP interface definition
  - It's an octopus
  - Example: the transfer from caged TM to accelerometer mode
  - Example: the alignment of TM in electrostatic and optical references
- Avoid complex transfer of (property of) hardware & software
  - There is always some work that falls through the cracks
  - Multi-level verification becomes an issue
- Hierarchical requirements: single stream

Case 2: requirements flow-down

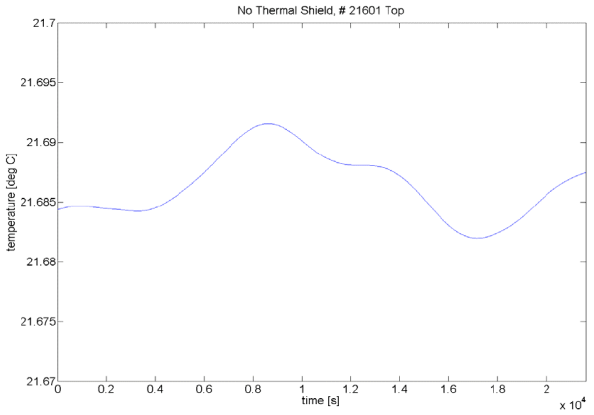
- Applicable requirements on LTP stem from ScRD, IRD –through the EID-A, GDIR, Product Assurance
- Example of requirement at box level (FEE)
  - **FEE-655/R**: *The actuation acceleration noise in the High Resolution Mode, caused by FEE SAU, shall be less than 1 x 10^{-14} $ms^{-2}/Hz^{1/2}$*
  - **FEE-671/IS-0400/T:** *The relative fluctuations of the AC actuation voltage amplitude at waveform carrier frequency, due to stability of DAC voltage reference, and measured at DVA output in the High Resolution Mode for peak amplitudes between 5V and 10V shall be less than 2ppm/$Hz^{1/2}$ in the extended frequency range between 0.3mHz and 30mHz*
  - **FEE-672/IS-0710 IS-0720/T:** *The actuation electronics voltage noise measured at DVA output in the High Resolution Mode shall be below 10mV/$Hz^{1/2}$ in the frequency range between 1mHz and 1Hz in the presence of any Science Mode AC or DC voltages (DC between 0 and ±5V)*
- Other performance requirements find verification difficult
  - Tip-off speed of TM: still debating on how to verify this requirement
  - Fluctuations of B field cannot be measured with existing techniques

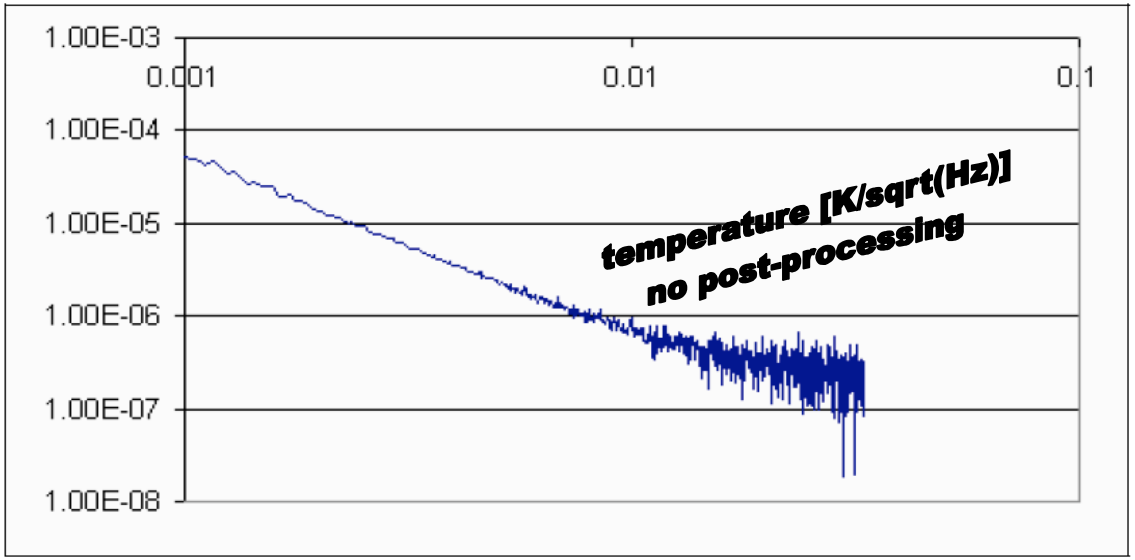
Lesson 2: requirement vs. verification

- The method of verification should be at the heart of each requirement
- Minimize verification by Analysis or Review (of design)
  - **Test!** (John Mather's talk at Symposium Dinner)
    - With procedure, a configured item, and quantified objectives
- Each hardware item, at each level of hardware development should be able to verify all (-most) of its requirements
  - Exception: avoid over-testing & over-handling
- Example 1: requirements for Electrode Housing development should only (mostly) consider mechanical requirements
- Example 2: requirements for FEE development should be measurable with a fluke

Case 3: PSD's for engineers

- LSD calculations for the thermal I/F between the LTP Core Assembly (LCA) based on input data (in the time domain)
- The purpose of this analysis is the comparison with and the evaluation of LSD calculations to support design work on the location of the LCA thermal shield

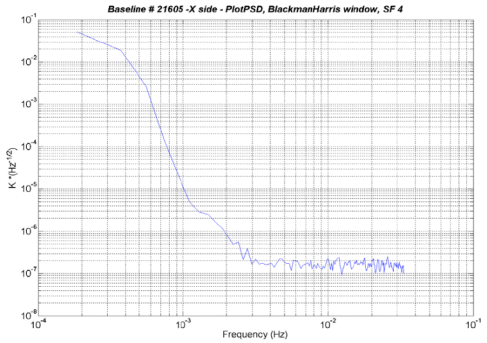




LSDs for same input data

- Default settings: PSD type "pwelch" with a smoothing factor of 10 (i.e. averaging input data) and a **Blackman window**
- Default settings. Input data vector is limited to 21,600 s (with an output step size of 15 s), smoothing is too strong and obviously not adequate for the number of input data, which is likely not sufficient for smoothing
- LSD w/o smoothing (SF = 1). The LSD shape now shows a behaviour, more typical for a thermal system, acting as a low-pass filter, with a 1/f shape
  - At the upper end of the LPF MBW numerical noise can be observed, which is related to the accuracy of the input data (in this case only 7 decimal places)
- A slight smoothing enables the LSD to show better identification of thermal stability numbers at certain frequencies
  - At the lower end of the MBW, the figure indicates a thermal stability is at 1x10-5 K/√ Hz

Let's open more windows



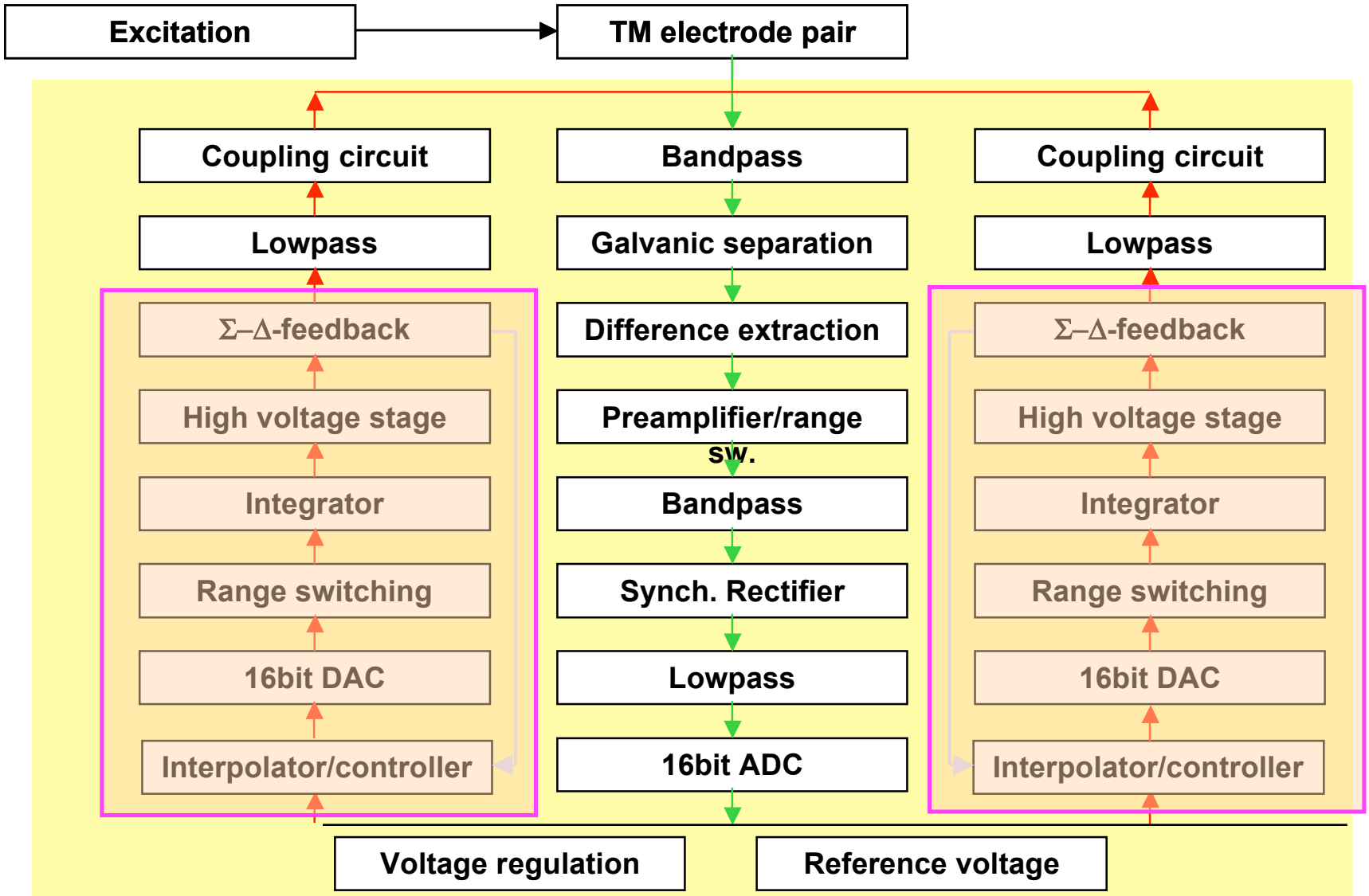
- And more windows…
  - The good guys: Hamming window, Tukey, Chebyshev, Parzen
  - The bad guys: No window, Flat Top window, Bartlett window
- Some windowing method may not be adequate for a certain type of input

Lesson 3: develop tools & methods

- Develop and certify standard tools and methods for
  - PSD analysis: tailoring to different domains might be necessary
  - Gravity data, analysis and verification
  - Magnetic field analysis and verification
  - Testing procedures
- Improve confidence in existing software tools
  - Large numbers, small numbers
  - Numerical instability or artifacts
  - FEM, thermal analysis
- If possible, reduce the learning curve of engineers and industrial teams by writing requirements in their own language

Case 4: 16 bit ADC - building blocks

Functional diagramm of FEE actuation function



Case 4: 16 bit ADC - building blocks

- A qualified >20-bit ADC (and DAC) would have simplified mode switching, and reduced noise in actuation Sigma-Delta loop
- A qualified hybrid for the ultra-stable, temperature compensated, voltage reference (for ADCs and DACs) would have improved actuation amplitude stability
- A qualified auto-zero, bipolar, operational amplifier would have reduced noise in sensing and actuation channels at low frequencies (<10mHz)
- A qualified high-impedance (FET), low noise and high-speed operational amplifier would have simplified sensing front-end design and reduced sensing noise
- A qualified hybrid for the sensor front-end, being a high impedance circuit, would have reduced mass & power, as well as improved performance (size matters)
- A qualified FPGA with ~million gates (e.g. RTAX-S series), would have provided more flexibility for a system on a chip design, and less mass (vs. RTSX-SU series, with <0.1 million gates)
- The acquisition chain could be simplified and SNR and offset problems relieved if the modulated carrier frequency is directly digitised and demodulation done numerically (this would have required a larger FPGA)

Lesson 4: qualify building blocks

- For the FEE, the most difficult requirement for LISA might be the actuation, in-band, noise floor of 1uV/rtHz @ 0.1mHz (TBC)
  - LTP requirement is 10uV/rtHz @ 1mHz and is difficult to achieve
- Evaluate, develop & qualify adequate components and circuitry
- Critically monitor on-going development
  - Application (mission critical?)
  - Environment
  - Usage (lifetime)
  - Schedule
- Look at vendor claims with inquiring eyes
- Get early your EEE parts expert or Product Assurance on-board

Case 5: mechanisms in LPF

- No mechanisms on LPF spacecraft during science operations
- Early technology development of Hold-down and Release Mechanism encountered “evolving” requirements
  - The ability to release the TM at very low tip-off speed and rate was added during the technology development
- The competitive selection process opted for a different technology
  - The TM interface to the mechanism was re-designed
  - The mechanism interface to the VE (Vacuum Enclosure) was re-designed
- The mechanism functions were split in three sub-mechanisms
  - Hold-down for ground and launch loads
  - Hold-down and pre-release in orbit
  - Low-speed release system
- Interfaces changed !

Lesson 5: on mechanisms

- Mechanisms are heavily dependent on configuration
- Be watchful of a design that was “qualified” for a “similar” application
- Be watchful of bread-boards: details matter

- Reminder: LISA Pathfinder has no mechanism in the optical path or inside the DFACS control loop during science mode
- Reminder: most mechanisms in orbit include SPF’s (single point failures), very often at mission level !
- If someone has an idea on how to remove the need for any mechanism, please heed his/her words

Case 6: performance prediction

- At LTP PDR, it was noted that performance analysis or resulting performance budgeting was mainly relying on earlier work by the science community
- The LTP Industrial Architect (ASD) had not performed independent analysis of requirements and could not present their own performance budget
- This issue was alleviated by
  - Overall Mission Performance engineering is performed by ASU
  - There was confidence in the work by the science community
- However, it became clear that ASD should have the capability to perform independent performance assessment
- So what should we do?
  - Perform a critical analysis of all the mathematical formulation needed to establish and monitor the LTP performance budgets, and get the corresponding formulation approved and configuration controlled
  - Create, validate and use an LTP performance model, based on the agreed mathematical formulation, to validate the adequacy and the current apportionment of performance requirements, the payload design, as well as to compile the predicted performance budgets from the test results throughout the LTP development lifetime.
- Yes, we are doing it

Lesson 6: transfer knowledge

- The science community has a wide and deep knowledge from ground installations, experimental metrology, theoretical work,…
- The "industrialisation" of this knowledge is key in order to develop a space mission that serves the purpose of the science community
  - This is applicable to LISA Pathfinder
  - Possibly so for LISA, too
- This is achieved through
  - The creation and maintenance of models steered to the development process of space missions
  - Fruitful communication between scientists and engineers
- Performance prediction goes from hardware details (FET design) to system overall performance ($3 \times 10^{-14}\ ms^{-2}/Hz^{1/2}$)

Case 7: performance verification

At LTP level we are defining (*apologies for the acronyms*):

- Engineering Model Tests
  - TRP OB, side walls, struts, EM Laser & DMU, set-up in a FM representative configuration (from mechanical & thermal point of view)
  - Test objectives: Verify OMS performance under vacuum, including thermal effects and influence from OBA mounting struts
  - Test set-up: Vacuum chamber (optically suitable), remotely controlled movable test mirrors for external adjustment
  - Option: connect with DFACS set-up for closed loop optical control of mirrors?
- Mechanical LCA (pre-)qualification for FM
  - Vibration test of a mechanically representative LCA setup
- OMS & DMU PFM Tests
  - Tests as the OMS EM test described above, but using the PFM units
- LCA PFM Tests
  - Vibration, shock and thermal tests: only a "go-no go" check of the OMS is possible due to the optical alignment of the TMs held by the CMA plungers
  - How do we know the TM has not been damaged along the way, desirably down to the launch pad?
  - How well can we measure the caged TM position via the IS FEE electrostatic sensing?
  - How can we practically check LCA internal alignment, desirably down to the launch pad?
- LTP End-to-end verification
  - Verification of the actuation function of the IS FEE in an integrated LTP configuration, through house-keeping parameters
  - A "go-no go" check of the discharging function to verify, at least, that the UV light arrives at the EH/TM

Lesson 7: sort out the testing now

- It is never too early to work on
  - Detailed descriptions of the tests, H/W and GSE configurations
  - AIT plan describing in detail documentation tree to be established for further definition of the AIT programme (e.g. test specs, procedures inputs for S/C level tests, etc).
  - The planning of the related preparatory activities
- Work out early facility requirements based on verification needs
- Plan the logistics
  - Money can be saved if equipment from other sources can be reused
  - Poor planning causes delays when it hurts most
- Engineers take requirements seriously (S. Vitale)
- The LPF business is the “creation of heritage”

Mid-way lessons learnt: Top Seven

1 Keep the hardware flow simple

2 Write requirements with their verification in mind

3 Develop and certify tools & methods (for engineers)

4 Qualify building blocks, design around qualified components

5 Watch out the mechanisms: they are configuration dependent

6 Transfer knowledge to engineers (and back?)

- Combine hardware performance with system performance

7 Sort out the testing early

In the near future…

- The need for mass and power **margins**
- The need for stress **margin**
- Vacuum maintenance
- Cleanliness through life cycle
- Physical and operational alignment
- Synchronisation of units
- Redundancy and performance
- Software validation
- End-to-End functional and performance analyses & tests
- GSE readiness
- Operations planning
- Commissioning & calibration runs
- …

- Thank you for being patient with LPF: we are hurrying up